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MIT-88T-56DBN

10G 802.3bt PoE Injector

1. INPUT :

- 1.1 Input Voltage: AC 100V ~ 240V
- 1.2 Input Frequency : 50 /60hz
- 1.3 Input Current: 1.21A at 100Vac @F.L
0.78A at 240Vac
- 1.4 Inrush current: 25A max at 120Vac & 60A max at 230Vac

2. OUTPUT :

2.1 Output Voltage & Current:

OUTPUT	56V
Max. load	1.34A
Power	75W
Min. Load	0A
Load reg. %	5%
Line reg. %	1%
Ripple %	1%
Noise %	2%

TOTAL POWER : 75 W



Note 1: Ripple & Noise bandwidth is from DC to 20Mhz. Terminated With a 47uF Capacitor and 0.1uf MPE Capacitor of Proper Polarity.

3. EFFICIENCY : 88% min. at AC 120V Input @F.L

4. PROTECTION

4.1 Short Circuit Protection

Output Short GND Terminal will not damage the Power Supply will Auto-Recover when Load status going to normally.

4.2 Over Voltage Protection : 59V ~ 65V

4.3 Over Current Limits : PSE Maximum Delivered Power, Per-Port(Table1 & 2)

4.4 LED indicates : JP2

4.5 Hold up time: 6mS min. at maximum load &120Vac Input.



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5.1 EMC: EN55032 Class B, FCC Class B

5.2 SAFETY: EN62368-1

6. GENERAL DESCRIPTION

6.1 Operation Temperature: -40 - +50 °C

6.2 Storage Temperature: -40 - +85 °C

6.3 Operation Humidity: 5% - 90%RH (non-condensing)

6.4 Cooling: Free air cooling

6.5 SIZE 90*118*40mm (L*W*H) DIN rail mountable

7.1 RJ45 pin assignment: @10G BASE

RJ-45 Input (Data Only)			RJ-45 Output (Data & Power)	
Pin	Symbol	Description	Symbol	Description
1	BI_DA+	Data Pair A+	-Vdc +BI_DA+	power(-)+Data Pair A+
2	BI_DA-	Data Pair A-	-Vdc +BI_DA-	power(-)+Data Pair A-
3	BI_DB+	Data Pair B+	+Vdc +BI_DB+	power(+)+Data Pair B+
4	BI_DC+	Data Pair C+	+Vdc + BI_DC+	power(+)+Data Pair C+
5	BI_DC-	Data Pair C-	+Vdc + BI_DC-	power(+)+Data Pair C-
6	BI_DB-	Data Pair B-	+Vdc +BI_DB-	power(+)+Data Pair B-
7	BI_DD+	Data Pair D+	-Vdc + BI_DD+	power(-)+Data Pair D+
8	BI_DD-	Data Pair D-	-Vdc + BI_DD-	power(-)+Data Pair D-
S	Shield	Shield	Shield	Shield

7.2 the input and output RJ45s with metal enclosure for shield, connected to FG.

8 INDICATOR :

8.1 LED1, 2 (RED) Indicate POE Output no valid detection.

8.2 LED1, 2 (GREEN) Indicate POE Output detected



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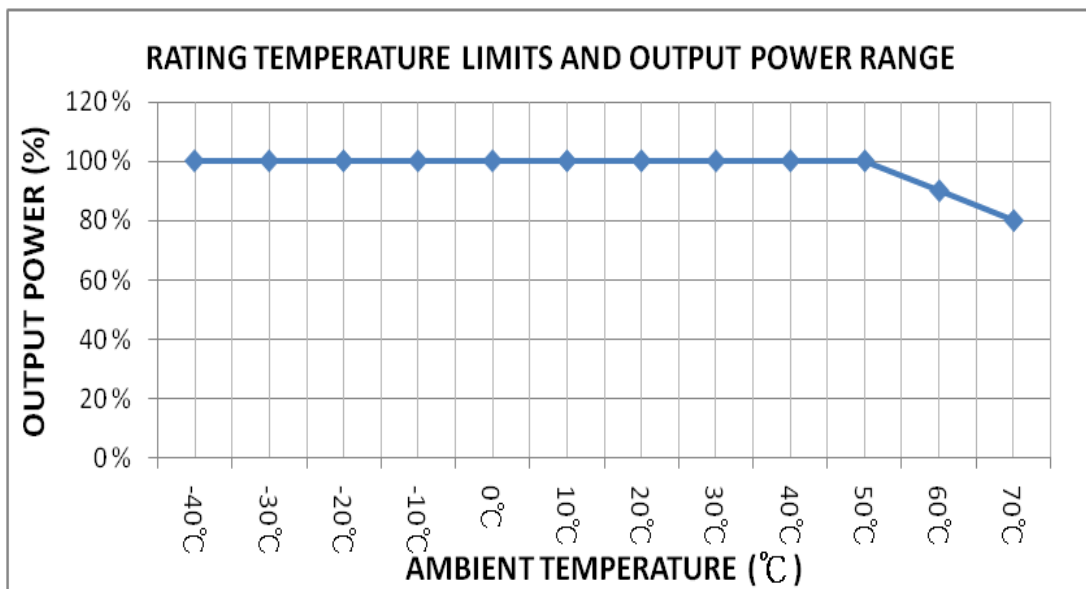
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Ambient	O/P Load
-40°C	100 %
-30°C	100 %
-20°C	100 %
-10°C	100 %
0°C	100 %
10°C	100 %
20°C	100 %
30°C	100 %
40°C	100 %
50°C	100 %
60°C	90 %
70°C	80 %





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LTC4291-1/LTC4292

APPLICATIONS INFORMATION

Table 1. IEEE-Specified Power Allocations, Single-Signature PD

PD CLASS	PSE OUTPUT POWER	ALLOCATED CABLING LOSS	PD INPUT POWER
1	4W	0.16W	3.84W
2	6.7W	0.21W	6.49W
3	14W	1W	13W
4	30W	4.5W	25.5W
5	45W	5W	40W
6	60W	9W	51W
7	75W	13W	62W
8	90W	18.7W	71.3W

BACKWARD COMPATIBILITY

The LTC4291-1/LTC4292 may be configured as an 802.3bt-compliant PSE, either Type 3 or Type 4. While 802.3bt PSEs cannot identify as an 802.3at Type 1 or Type 2 PSE, there is no loss in PSE functionality; all 802.3bt-compliant PSEs are fully backwards compatible with existing 802.3at Type 1 and Type 2 PDs as shown in Table 2. In addition to full compatibility, 802.3bt PSEs extend support for lower standby power, enhanced current limit timing, and dynamic power management to all PD Types (as supported by the PD application).

Table 2. PSE Maximum Delivered Power, Per-Port

DEVICE	PSE					
	STANDARD	TYPE	802.3at			
			1	2	3	4
PD	802.3at	1	13W	13W	13W	13W
		2	13W*	25.5W	25.5W	25.5W
	802.3bt	3	13W*	25.5W*	51W	51W
		4	13W*	25.5W*	51W*	71.3W

*Indicates PD allocated less power than requested.

Software register map compatibility with LTC4266 and LTC4271-based PSEs has been maintained to the extent possible. LTC4291-based PSEs utilize two channels to control a single PSE port. This multiplicity of channel status and control requires extensions to the existing register map.

For register map details please contact Analog Devices to request the LTC4291 Software Programming documentation.

Special Compatibility Mode Notes

- As with prior generations, each I²C address provides status and control for four PoE ports. Each port register slice provides port control and status as well as channel A vs B control and status.
- Certain status registers, e.g. Port Status and Power Status, relate to a channel state, as opposed to port state and are split into three copies; a generalized port state, channel A state and channel B state.
- Certain command registers, e.g., Power-on pushbutton, likewise are bifurcated to allow per-channel control.

OPERATING MODES

The LTC4291-1/LTC4292 includes four independent ports, each of which can operate in one of three modes: manual, semi-auto, or auto. A fourth mode, shutdown, disables the port (see Table 3).

Table 3. Operating Modes

MODE	AUTO PIN	OPMD	DETECT/CLASS	POWER-UP	AUTOMATIC THRESHOLD ASSIGNMENT
Auto	1	11b	Enabled at Reset	Automatically	Yes
	0	11b	Host Enabled	Automatically	Yes
Semi-auto	0	10b	Host Enabled	Upon Request	No
Manual	0	01b	Once Upon Request	Upon Request	No
Shutdown	0	00b	Disabled	Disabled	No

In manual mode, the port waits for instructions from the host system before taking any action. It runs a single detection, or detection and classification cycle when commanded to by the host, and reports the result in its Port Status register. The host system can command the port to apply or remove power at any time.

In semi-auto mode, the port repeatedly attempts to detect and classify any PD attached to it. It reports the status of these attempts back to the host, and waits for a command from the host before applying power to the port. The host must enable detection and classification.



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LTC4291-1/LTC4292

APPLICATIONS INFORMATION

Auto mode operates the same as semi-auto mode except it will automatically apply power to the port if detection and classification are successful. Auto mode will autonomously set the I_{CUT-2P} , I_{LIM-2P} , and P_{CUT-4P} values based on the Class result. This operational mode may be entered by setting AUTO high at reset or by changing the OPMD state to Auto. See Auto Mode Maximum PSE Power section.

In shutdown mode the port is disabled and will not detect or power a PD.

Regardless of which mode it is in, the LTC4291-1/LTC4292 will remove power automatically from any port and/or channel, as appropriate, that generates a fault. It will also automatically remove power from any port/channel that generates a disconnect event if disconnect detection is enabled. The host controller may also command the port to remove power at any time.

Reset and the AUTO Pin

The initial LTC4291-1/LTC4292 configuration depends on the state of AUTO during reset. Reset occurs at power-up, whenever RESET is pulled low, or when the global Reset All bit is set. Changing the state of AUTO after power-up will not change the port behavior of the LTC4291-1/LTC4292 until a reset occurs.

Although typically actively managed by a host controller, the LTC4291-1/LTC4292 may alternatively be configured for autonomous operation by setting AUTO high. With AUTO high, each port will detect and classify repeatedly until a PD is discovered, set I_{CUT-2P} , I_{LIM-2P} , and P_{CUT-4P} according to the PSE assigned Class, apply power to valid PDs, and remove power when a PD is disconnected.

Tables 4 and 5 show the I_{CUT-2P} , I_{LIM-2P} , and P_{CUT-4P} values that will be automatically set in auto mode, based on the PD requested Class.

Table 4. Typical Auto Mode Power On Thresholds, Single-Signature PD

CLASS	PER-CHANNEL		PER-PORT
	I_{CUT-2P}	I_{LIM-2P}	P_{CUT-4P}
1	94mA	425mA	5.43W
2	150mA	425mA	8.69W
3	338mA	425mA	19.5W
4	638mA	850mA	36.4W
5	581mA	850mA	52.7W
6	731mA	850mA	70.0W
7	825mA	1063mA	87.4W
8	975mA	1167mA	96.6W

Table 5. Typical Auto Mode Power On Thresholds, Dual-Signature PD

CLASS	PER-CHANNEL		
	I_{CUT-2P}	I_{LIM-2P}	P_{CUT-2P}^*
1	94mA	425mA	5.43W
2	150mA	425mA	8.69W
3	338mA	425mA	19.5W
4	638mA	850mA	36.4W
5	975mA	1167mA	48.3W

*A per-port P_{CUT-4P} threshold holds the sum of P_{CUT-2P} for each powered channel.

CONNECTION CHECK

Connection Check Overview

IEEE 802.3bt introduces a new detection subroutine known as connection check. A connection check is required to determine whether the attached PD is a single-signature PD, a dual-signature PD or an invalid result.

In 802.3at, only one PD configuration was described; this is known as a single-signature PD and is shown in Figure 10. A single-signature PD presents the same 25k detection resistor to both the pairsets in parallel.

New in 802.3bt is the dual-signature PD as shown in Figure 11. A dual-signature PD presents two fully independent 25k detection signature resistors, one to each pairset.